

Oxide-encapsulated vertical germanium nanowire structures and their DC transport properties

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Abstract

We demonstrate the p-type doping of Ge nanowires (NWs) and p–n junction arrays in a scalable vertically aligned structure with all processing performed below 400 °C. These structures are advantageous for the large scale production of parallel arrays of devices for nanoelectronics and sensing applications. Efficient methods for the oxide encapsulation, chemical mechanical polishing and cleaning of vertical Ge NWs embedded in silicon dioxide are reported. Approaches for avoiding the selective oxidation and dissolution of Ge NWs in aqueous solutions during chemical mechanical polishing and cleaning of oxide-encapsulated Ge NWs are emphasized. NWs were doped through the epitaxial deposition of a B-doped shell and transport measurements indicate doping concentrations on the order of 10^{19} cm^{-3} .

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Germanium nanowires (NWs) are being actively investigated for various applications including field effect transistors [1, 2] and p–n junction devices [3]. However, much of the work with Si NWs [4–6] and all the Ge NW devices in the literature that we are familiar with has been limited to individual devices lying horizontally on a substrate. These devices may not be feasible for the large scale integration of high density circuits due to the extended processing necessary for aligning, contacting, and integrating such NW components. Efficient and scalable methods are necessary for the large scale assembly and integration of NWs for different device architectures.

Vertically aligned NWs and carbon nanotubes (CNTs) have been proposed to provide an efficient, reproducible route to ultrahigh density nanoscale device arrays. These structures

have been demonstrated in Si NW surround-gate field effect transistors [7, 8], CNT interconnects [9], CNT electrochemical sensors [10], and CNT field emission displays [11]. This architecture of extension into the third dimension may provide ultrahigh density devices for scaling transistors, memory, logic, sensors, or programmable vias. The resulting dense verticals arrays also offer unique advantages for applications such as field emission devices [11], three-dimensional integrated circuits [9], and photovoltaics [12, 13].

Germanium is a promising material for NW devices because of the low temperatures (<400 °C) required for its growth and doping [14–16], its high intrinsic electron and hole mobilities compared with Si [17], large excitonic Bohr radius of about 24 nm [18], and compatibility with Si-based integrated circuit fabrication. However, research on Ge NW device fabrication has been limited, especially in comparison to that on CNTs and Si NWs, in part as a result of the chemical instability of Ge surface oxides. This presents

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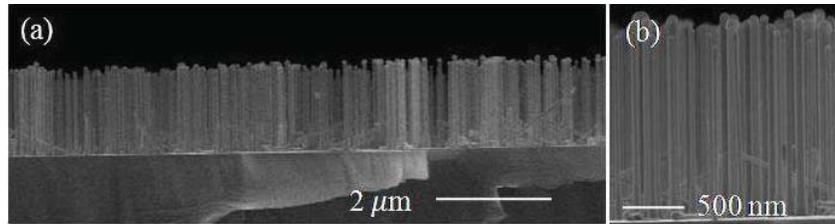


Figure 1. Cross-section SEM of 60 nm diameter Ge NWs grown on Ge(111) substrates. (a) Illustrates that most of the NWs are vertical across the entire wafer. (b) Shows that the NWs are uniform in diameter.

a particular challenge for the fabrication of vertical NW structures, many of which require insulator encapsulation and subsequent chemical mechanical polishing (CMP) to planarize the structure and expose the NW tips to synthesize top contacts [7–10]. Encapsulation of vertical nanostructures may be done both to provide greater mechanical and chemical stability during device fabrication and to electrically isolate the final devices from one-another. The encapsulation layer should conform to the surfaces of the high-aspect-ratio nanostructure array, and its deposition should not adversely affect device performance. Therefore, low temperature and conformal oxide deposition processes are highly desirable.

While CMP is widely used in microfabrication, there are limited reports on its application to Ge devices [19–22]. Not only are Ge oxides chemically reactive, but the amount of Ge present in NW arrays is very small. Therefore, there is a need to develop a CMP and post-CMP cleaning process with minimal Ge etching. Most silicon oxide CMP slurries are based on NaOH, KOH, or NH₄OH-containing solutions with pH > 10 [23]. However, Ge reacts preferentially with hydroxyl ions and the resulting oxide dissolves readily in basic aqueous solutions [24]. Aqueous solutions containing oxidants etch Ge readily because GeO₂ is soluble in water and is reported to dissolve at a rate of about 2 μm min⁻¹ at 25 °C [25]. A number of studies on the CMP and post-CMP cleaning of SiGe layers have been reported previously in the literature [19–22]. However, most of these structures had low Ge content (under 30%), as Ge tends to react with the hydrogen peroxide present in Standard Clean 1 (SC1) solutions (NH₄OH/H₂O₂/H₂O) often used in the post-CMP cleaning of silica surfaces [20]. There have been a few reports of the successful planarization of higher Ge composition SiGe alloys [19, 20] and to our knowledge, only one account of CMP of pure Ge [25]. However, these reports describe the planarization of bulk Ge substrates and are concerned with the etching of Ge mostly as it influences surface smoothness.

In this paper, we report an efficient, reproducible process for the directed fabrication of large arrays of vertically aligned Ge NW structures, with all processes performed at temperatures less than 400 °C. Parallel arrays of NWs are desirable in certain applications since they increase total current and increase signal-to-noise ratio, though single vertical NW devices may also be fabricated by using e-beam lithography to pattern catalysts. The NWs are aligned through epitaxial vertical growth by low temperature, Au-catalyzed chemical vapor deposition (CVD) via the vapor–liquid–solid

(VLS) mechanism. The vertical Ge NWs may be boron doped to fabricate p–n junction arrays. The NWs were encapsulated in oxide by an alternating layer deposition process, and this is compared with oxide deposition by plasma enhanced CVD (PECVD). The oxide-encapsulated vertical Ge NWs can be polished to produce a stable array with NW tips exposed for making electrical contact. The planarization procedure involves the use of an acidic slurry and only DI water for the post-CMP cleaning. Our vertical Ge NW arrays can be doped through the deposition of an epitaxial B-doped Ge shell and used to form p–n junctions with underlying n-type substrates.

2. Fabrication process

Details of the fabrication process can be found in the appendix. Gold colloids of 40 nm nominal diameter were deposited on top of low resistivity p-type Ga-doped (111) Ge wafer pieces ($\rho < 0.1 \Omega \text{ cm}$) and n-type Sb-doped Ge wafer pieces ($\rho < 0.08 \Omega \text{ cm}$) by adding 1% HF to the Au colloid solution for a concentration of 0.1 M HF and depositing for 60 s [26]. The NWs were grown in a cold-wall CVD reactor using GeH₄ and H₂ gases and a two-temperature growth process. Figure 1 shows the cross-section scanning electron micrograph (SEM) of the NWs, where (a) illustrates that most (>80%) of the NWs are vertical and (b) demonstrates that the NWs are mostly uniform in diameter. As previously reported, the two-step temperature growth process leads to NWs with uniform diameter and epitaxial to the $\langle 111 \rangle$ directions of the substrate with a very strong preference for vertical growth, compared to growth along the $\langle 111 \rangle$ axes that are inclined relative to the substrate normal [16, 26].

Among 100 NWs grown, the intrinsic NWs are $60 \pm 10 \text{ nm}$ in diameter, where a Gaussian function was fit to the diameter distribution and \pm refers to one standard deviation [27]. The variation in NW diameter results from Au diffusion on the substrate surface. The NWs have minimal taper because most of the deposition takes place at a temperature of 300 °C, at which the uncatalyzed, sidewall decomposition of the GeH₄ precursor is relatively slow [16]. The Ge NWs are doped by the deposition of a thin shell of B-doped Ge using GeH₄, H₂, and B₂H₆ [3]. Figure 2(a) shows the Ge NWs after the deposition of a B-doped homoepitaxial shell of about 20 nm in thickness so that the NWs are now about 100 nm in diameter. Figure 2(b) illustrates the doped NWs diameter. Continued deposition of

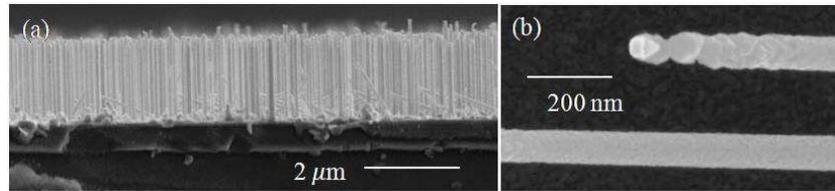


Figure 2. Doped shell NWs after p-type shell deposition. (a) Cross-section SEM image of the doped core shell NWs. (b) Planar SEM image of the doped shell NWs. There is some precipitation out of the Au catalyst during the thin film deposition step. The NWs are now about 100 nm in diameter, indicating a shell of about 20 nm thickness.

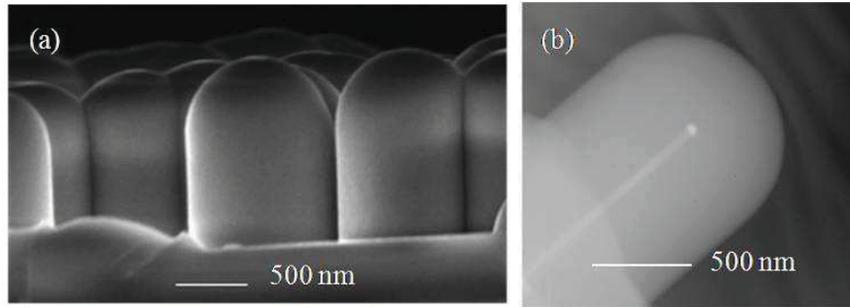


Figure 3. Deposition of silicon oxide around Ge NWs. (a) cross-section SEM of Ge NWs after alternating layer deposition of 50 cycles TMA and silanol; (b) TEM image of one of the vertical Ge NWs inside the SiO₂ dielectric shell.

Ge from the catalyst is evident in the lengthening of the NWs during doped shell deposition.

Silica was then deposited around these vertically aligned Ge NWs to encapsulate and isolate the NWs and provide structural stability. Figure 3 shows the results on alternating layer deposition of silicon dioxide around Ge NWs. We have compared oxide deposition by an alternating layer deposition process [28] and a PECVD process to encapsulate the NWs. Figure 3(a) shows a cross-section SEM after approximately 50 cycles of trimethylaluminum (TMA) and silanol exposure. We observe that a uniform surface coating is deposited around each NW, and that the NWs remain vertical after deposition. The silica is very conformal even where the NWs are relatively dense. We observe that there is a one-to-one correspondence between ‘domes’ and single NWs by tracking NWs as SiO₂ was progressively deposited on the sample and by cross-section TEM. Figure 3(b) shows the cross-section TEM image of a single Ge NW embedded inside an SiO₂ shell. The manner in which the coatings on two or more adjacent wires coalesce to form an embedding coating suggests that the encapsulation of high density areal densities of vertical NW devices should be possible with these coatings. We also deposited oxide around NWs by PECVD, which resulted in somewhat less conformal deposition. In particular, shadowing results in more silica deposition at the tops of the NWs relative to lateral deposition onto the two different sidewalls. Further details and comparisons of the two different oxide deposition processes can be found in appendix.

The samples were subsequently polished by CMP [29] to planarize the surface and expose the Ge NW tips. The Au particles at the tips of the NWs were removed during this procedure. This also improves the complementary metal

oxide semiconductor compatibility of the fabrication process, because Au is a deep carrier trap state that acts as an efficient generation/recombination center that reduces minority carrier lifetime and increases pn junction leakage. The polishing process removed some of the SiO₂ encapsulation and the tops of the Ge NWs, without affecting the epitaxy and vertical alignment, resulting in a planar structure of SiO₂. The main difficulty in the CMP of these structures is that the process must remove SiO₂ with a minimal amount of Ge etching, so that the tips of the Ge NWs are exposed and can be contacted electrically. In order to evaluate the etching of various slurries, we immersed freestanding Ge NW samples grown on Si(111) substrates in various slurries for 20 min at room temperature. The etch rate of Ge in acids is not appreciable [30] and we determined that an acidic slurry etched the Ge minimally. In particular, we used the Ultra-Sol™, 7H slurry with silica particles of 60–80 nm, a pH of 2.3, and 30% solids. We polished the NW samples until the NWs were approximately 600 nm in length as measured by ellipsometry.

Post-CMP cleaning is important to remove slurry silica particles and chemical contamination of the surface from our samples. Post-CMP cleaning for the removal of silica slurry residues on silicon oxide is often done using a standard SC1 clean (NH₄OH/H₂O₂/H₂O) [23, 29]. The polishing of SiGe buffer layers has also used this type of clean [20–22]. We considered the effects of an SC1 clean. Figure 4(a) shows a planar SEM image of our sample after an SC1 clean of 2:3 NH₄OH (28–30% NH₃): 30% H₂O₂. With this post-CMP cleaning process, the Ge NWs were etched away leaving high-aspect-ratio holes as indicated by the black features in the micrographs. The holes are about 60 nm in diameter, which is the nominal diameter of the colloid-grown intrinsic

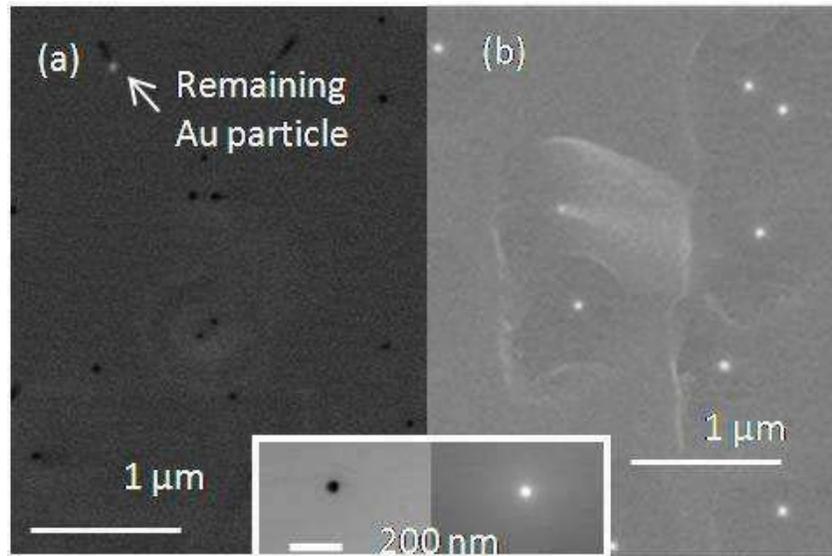


Figure 4. CMP of silicon oxide around Ge NWs. (a) Plan-view SEM of sample using a post-polish SC1 clean where the Ge NWs are etched away, (b) plan-view SEM of sample using a post-CMP clean by megasonic agitation and scrubbing with a PVA sponge where the Ge NWs are left intact. The insets show a zoomed in image of a single hole or wire tip, which is about 60 nm in diameter.

Ge NWs. Hydrogen peroxide is reported to disassociate to form O_2H^- ions that attach to Ge ions to form the surface complex $Ge(OH)_2^{++}$. These Ge hydroxyl complexes are removed from the Ge surface by reaction with water to form H_2GeO_3 (aq) [24]. The Au catalyst particles can be observed by SEM at the end of some of the tilted epitaxial Ge NWs, where the SC1 solution has etched away the Ge NW trailing behind the Au. These processes result in very fast etching rates for Ge(s) in peroxide containing aqueous solutions. The dissolution rate of $1 \text{ mg cm}^{-2} \text{ h}^{-1}$ (or 30 nm min^{-1}) for 30% H_2O_2 in 25°C reported by Cerniglia *et al* [24] (the lowest dissolution rate reported in that paper and that we have found in the literature) is too high for SC1 solutions to be of practical use in post-CMP cleaning of our Ge NW samples. Aqueous solutions containing oxidants will have high etch rates for Ge because of the high etch rate of GeO_2 in H_2O .

While the SC1 clean is inadequate for cleaning the Ge NW samples, the etch rate of Ge in DI H_2O is about $0.0007 \text{ nm min}^{-1}$ [30]. In order to clean our samples, we have, therefore, adopted a scrubbing method using only DI H_2O as a cleaning solution. Figure 3(b) shows images obtained after a combination of ultrasonic agitation and brush scrubbing of the encapsulated NW samples. Ultrasonic agitation in DI water for 2 min followed by scrubbing with a polyvinyl alcohol (PVA) sponge for 2 min with several kg cm^{-2} of force to remove the silica particles was found to be effective. The combination of the non-contact frequency pressure waves in agitation and the mechanical and electrostatic effects of sponge scrubbing were found to remove the silica particles of the CMP slurry from the sample surface, while leaving the Ge NWs intact and the sectioned tips exposed.

3. DC electrical transport results

A 4 nm Ti sticking layer and thin Pd films of 40 nm nominal thickness were deposited on top of these Ge NW structures to form top metal contacts. The $I-V$ results obtained are for NWs that have been embedded in the PECVD-grown oxide. Figure 5(a) shows the $I-V$ characteristics of undoped Ge NWs and (b) p-type doped shell Ge NWs on top of p+ Ge substrates. The intrinsic NWs exhibit some nonlinearity in the $I-V$ curves, similar to what has been observed in Si NWs [31], though the present curves are asymmetric.

The current data have been normalized on an approximately per-NW basis as determined from large-area SEM images. The data shown here are for Pd pads roughly $(30 \mu\text{m})^2$ in area with a few hundred NWs under the pads. For the purposes of clarifying the subsequent discussion of p-n junction devices, we use the convention that the forward bias direction refers to a positive voltage applied at the top electrode relative to the substrate and vice versa. In the actual measurements, the probe tip was grounded while the substrate was biased. The general features of the intrinsic NW $I-V$ curves shown in figure 5(a) are consistent with Schottky barrier-limited conduction of electrons across the top metal/Ge interface under forward bias and top metal/Ge junction leakage current under negative bias. Under forward bias, the current is limited by the Schottky barrier seen by electrons. The Fermi level of most metals in contact with Ge is reported to be pinned close to the valence band edge [32] and the Ge/Pd junction has been reported to have a Schottky barrier height of 0.65 eV [33]. The intrinsic NWs show a similar exponentially increasing current with reverse bias. We believe this is a consequence of thermionic field emission and field emission through the Pd/Ge Schottky barrier. Ge surfaces exhibit a substantial density of states in the

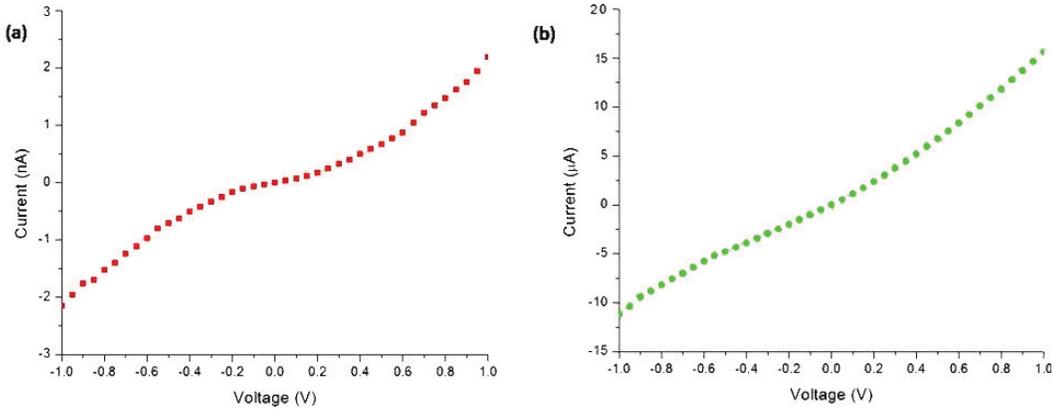


Figure 5. (a) I - V curve of an undoped 60 nm diameter NW on p-type substrate. (b) I - V curve of a doped shell 100 nm diameter NW on p-type substrate.

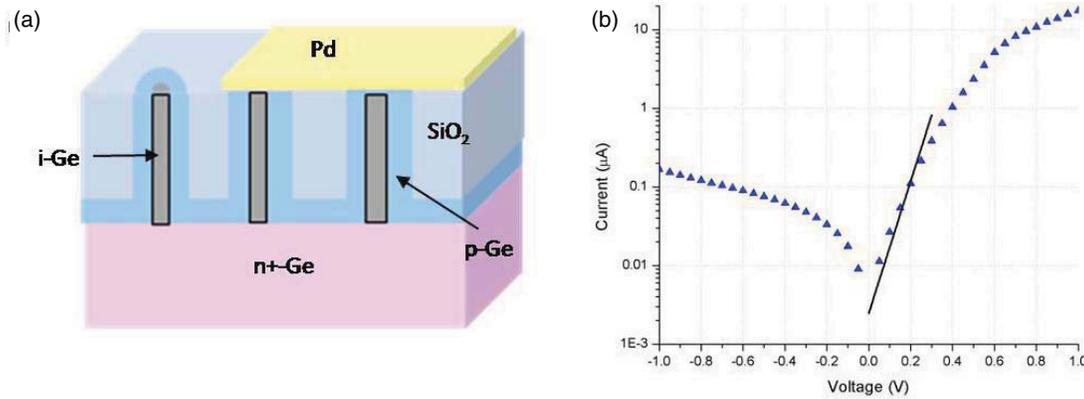


Figure 6. (a) Schematic of our doped shell NW structure on top of an n-type substrate. (b) I - V curve of a doped shell 100 nm diameter NW on n-type substrate.

band gap [34] and the CMP process may also contribute to defect states on the NW tip surface. These states are expected to facilitate the tunneling of current through the Schottky barrier under reverse bias. For the p-doped NWs, the I - V curves are closer to linear, suggesting the metal electrodes make ohmic contacts to the p-type Ge NWs. There is some slight nonlinearity in the p-type NWs in the reverse bias direction, most likely due to defect or gap states at the top Pd/Ge contact.

To quantify the dopant concentration of the Ge NW shell and the intrinsic NW, we calculated the resistivity of these NWs, assuming bulk hole mobility at room temperature and negligible contact resistance, along with estimates of the number of NWs from SEM images. We used only the nominal cross-sectional area of the doped shell for the estimates of current density in the doped NWs, because the main channel for dopant incorporation in Ge NWs is reported to take place through the NW surface and not through the catalyst by incorporation during VLS mechanism at the shell deposition temperature we employed [3]. For the intrinsic NWs, we estimated $\rho \approx 10 \Omega \text{ cm}$, and for the p-type doped shell NWs, $\rho \approx 0.001 \Omega \text{ cm}$. Assuming bulk Ge electron and hole mobility values [35], these resistivities correspond to carrier

concentrations of $\approx 10^{14} \text{ cm}^{-3}$ and $\approx 10^{19} \text{ cm}^{-3}$, respectively. The active dopant concentration in the doped shells was similar to results obtained in measurements on planar Ge thin films deposited on oxide-coated Si wafers, samples on which no Au catalyst particles were present, under the same CVD conditions. A typical active B dopant concentration in these planar films is approximately 10^{19} cm^{-3} .

Recently, a linear Ge NW p-n junction has been demonstrated [3]. Most research reported on p-n structures has been limited to individual horizontal NW devices [3, 36]. We have studied an efficient method to prepare large arrays of vertically oriented p-n Ge NW junctions, where the junction is formed between the NW and the substrate. Figure 6(a) shows a schematic of the device layout. We have grown NWs on n-type Ge(111) substrates with a resistivity of $< 0.01 \Omega \text{ cm}$. When the Ge NWs are grown on doped n-type substrates, we note that the NWs exhibit rectifying p-n junction behavior. For the p-type doped shell Ge NWs, there is a notable increase in current under forward bias as well as linearly increasing negative current under reverse bias. This behavior can be explained by the thermal generation current of carriers. Under reverse bias, the thermal generation current increases linearly

as the width of the p–n junction depletion region increases. During the deposition of B-doped Ge shell around the NWs, a thin film of B-doped Ge is also deposited on the Ge substrate. This thin film forms a p–n junction with the underlying n-type substrate along its entire surface and encapsulates any of the unreacted Au catalyst particles remaining on the substrate surface. The Au catalysts or defects at this interface could potentially lead to the significant generation of reverse bias current. We also note that because there are several hundred NWs in parallel, this leakage current may result from only a few NWs or leakage paths.

We provide a fit to our data using the ideal diode equation, $I = I_0 e^{\left(\frac{V_d}{nV_T}\right)}$, where V_d is the applied voltage, n is the ideality factor, and V_T is the thermal voltage, which is ≈ 26 mV at 300 K. In figure 6(b), we plotted our fit for $n = 2$ for the data from $V_d = 0.05$ to 0.3 V. $n = 2$ is the ideality factor for a p–n junction where the forward current is dominated by recombination [37]. $I_0 = 3$ nA for the doped shell NW. The best fit of n for the curves is $n \approx 3$. The plot indicates a decrease in the slope of the log scale I – V plots under higher forward bias which appears to result from the series resistance limiting the current.

4. Summary

We have demonstrated a potentially scalable fabrication process for producing large arrays of vertical Ge NWs for device purposes. Effective encapsulation of dense arrays of vertical nanowires using SiO₂ deposited by either alternating layer deposition or plasma enhanced CVD was performed. We have demonstrated a CMP and post-CMP procedure for planarizing these embedded Ge NW structures to expose the tips of the NWs. An acidic slurry was used to minimize etching of Ge during the polishing process. Standard post Si-CMP cleans were inadequate for cleaning Ge NW samples as they etched away the Ge NWs very quickly, and we have instead developed a combination non-contact and contact process using only DI H₂O. The CMOS incompatible Au catalyst was also removed from the nanowire tips during the CMP process. While the dissolution of Ge was not desirable in the present case, the observed selectivity of the aqueous etching Ge NWs may be potentially useful for other catalytic or nanofluidic applications. As demonstrated in this work, Ge NWs can be used as templates for the deposition of dielectric or semiconductor materials, and then the Ge can be subsequently etched away. Finally, we have demonstrated the p-type doping of vertical Ge NW structures with $p \approx 10^{19}$ cm⁻³. The Ge NW arrays can be used to form vertical p–n junctions with rectifying behavior. All fabrication processes studied took place at temperatures below 400 °C, which may be important for preserving the performance of integrated nanodevices.

Acknowledgments

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Appendix. Fabrication process details

Our vertical Ge NW structures are fabricated according to the following general procedure. Figure A.1 gives an overview of the fabrication process flow. 40 nm uniform-diameter Au colloids were deposited on top of a doped (111) Ge wafer. Ge NWs were individually grown from these Au colloids and are epitaxial to the underlying substrate. Silica was deposited around the Ge NWs. The structure was then planarized by CMP to expose the tips of the Ge NWs. We deposited top metal electrodes for DC electrical transport characterization of the vertical Ge NWs. Figure 1(a) shows the cross-section scanning electron micrograph (SEM) of the NWs.

A controlled (111) orientation of the NWs was obtained by their epitaxial growth on the single-crystalline substrate [16]. The Ge NWs used in this study were grown using colloidal gold particles (BB International, nominal particle diameter 40 nm) as the catalysts. p-type Ga-doped (111) Ge wafer pieces ($\rho < 0.1$ Ω cm) and n-type Sb-doped Ge wafer pieces ($\rho < 0.08$ Ω cm) were used as the substrates. All of the substrates were cleaned using an UV ozone process for five minutes prior to colloid coating of the wafer surface. 1% HF was added to the Au colloid solution for a concentration of 0.1 M HF and deposited for 60 s by dip coating [26]. NW growth was carried out in a cold-wall, lamp-heated, chemical vapor-deposition chamber, with a GeH₄ precursor flow of 6.7 sccm, H₂ flow of 460 sccm, and a total pressure of 30 Torr. A two-temperature growth procedure was used for the growth of NWs, details of which are described elsewhere [38]. The Ge substrates were heated to 375 °C for 2 min and then immediately cooled within 90 s to 300 °C where they are kept for 18 min. As previously reported [16], the two-temperature procedure leads to the growth of GeNWs that have uniform diameter and are epitaxially aligned parallel to the (111) directions of the substrate with a very strong preference for vertical growth, compared to epitaxial growth along the (111) axes that are inclined relative to the substrate normal [16, 39]. The average diameter of the NWs is 60 nm.

In order to dope the NWs, simply flowing B₂H₆ during the growth process tends to lead to tapered Ge NWs and it is questionable whether B is incorporated through the catalyst [40]. Instead, we found that we could dope the Ge NWs by the deposition of a thin shell of B-doped Ge similar to the process reported in Tutuc *et al* [3]. The doped shell was deposited with a precursor 2 sccm, H₂ flow of 418 sccm, and a B₂H₆ flow of 0.03 sccm with a total pressure of 10 Torr. The shell was deposited at 375 °C for 10 min, and resulted in a homoepitaxial shell of about 20 nm in thickness, so that our NWs are now about 100 nm in diameter. We obtained NWs

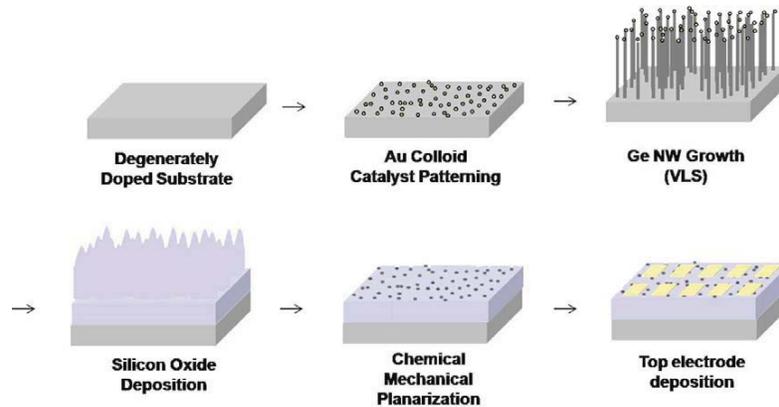


Figure A.1. Schematic of our fabrication process.

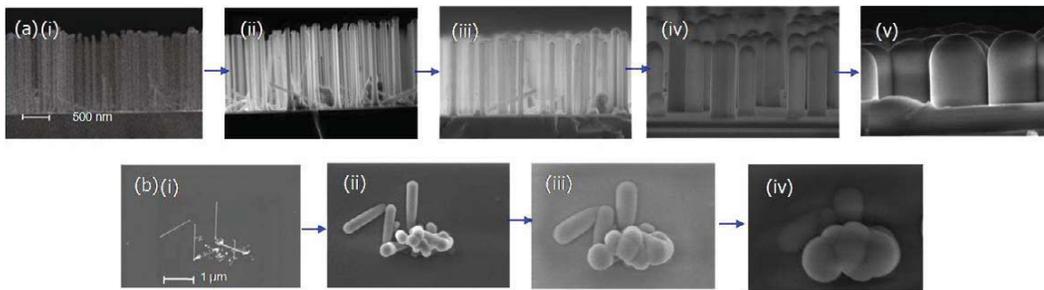


Figure A.2. Results from the deposition of silica around Ge NWs. (a) Cross-section SEM images of Ge NWs, after deposition of silica by alternating layer deposition for (i) original NWs, (ii) 1 cycle, (iii) 5 cycles, (iv) 20 cycles, and (v) 50 cycles of TMA and silanol showing progressive increase in the thickness of SiO₂ shells. (Images courtesy of Hemant Adhikari) (b) Plan-view SEM images of the same cluster of Ge NWs, with a progressive increase in the thickness of SiO₂ shells around the NWs using PECVD oxide for (i) original NWs, (ii) 200 nm, (iii) 500 nm, and (iv) 1000 nm of SiO₂. The silica deposits conformally around the NWs so that there is a single dome for each NW. As more silica is deposited, these domes merge together.

of uniform diameter by using this second thin film deposition stage. The doped shell deposits at $\approx 2 \text{ nm min}^{-1}$. There is some continued growth of the NW tip during this deposition process.

Figure A.2 shows the main results of deposition of silicon oxide around Ge NWs. We have compared oxide deposition by an alternating layer deposition process [28] and a PECVD process to encapsulate the NWs. Figure A.2(a) shows a cross-section SEM after approximately 50 cycles of trimethylaluminum (TMA) and silanol. We observed that a uniform surface coating is deposited around each NW, and that the NWs remain vertical after deposition. The silica is very conformal even where the NWs are fairly dense and we observed there is a one-to-one correspondence between ‘domes’ and single NWs by tracking NWs as SiO₂ was progressively deposited on the sample and by cross-section TEM. Figure A.2(b) shows the cross-section TEM image of a single Ge NW embedded inside an SiO₂ shell. The manner in which the coatings on two or more adjacent wires coalesce to form suggests that the high density embedding of vertical NW devices should be possible with these coatings.

The PECVD oxide was deposited at 350 °C at 650 mTorr with 1400 sccm N₂O and 400 sccm 2% SiH₄. The deposition

rate of the PECVD oxide is about 36 nm min^{-1} . The films of aluminum-doped silica were deposited by an alternating layer deposition process. This coating method offers the benefits of atomic layer deposition (ALD), such as control over dielectric composition and structure and uniform film thickness over large areas and in convoluted geometries, while also having deposition rates much faster than ALD. Therefore, it allows for encapsulation of the vertical NWs in a practical time-frame. The aluminum catalyst layer was formed by pulses of trimethylaluminum [TMA, Me₃Al] vapor, with a solid TMA precursor temperature of 28 °C. Silica was formed from the vapor of tris(tert-butoxy)silanol [TBOS, (t-BuO)₃SiOH] heated at 125 °C, at which temperature it is a liquid (melting point 65 °C). The substrate temperature was kept at 250 °C. Vapor doses of TMA and TBOS were supplied to the heated substrate in alternating pulses, with three doses of TMA for each dose of TBOS comprising one cycle. Nitrogen was used as a purge gas between the pulses. The dose of TBOS for each cycle is about 200 mol and the resulting surface exposure from the each dose is 3×10^7 Langmuir. It has been shown that many optical, electrical, and mechanical properties of the silica layers are hardly changed by the presence of the small amount of alumina [28]. The refractive index, dielectric constant,

leakage current, and breakdown voltage are similar to values measured for pure silica films grown thermally on silicon.

Figure A.2(a) shows SEM images of vertically aligned NWs after SiO₂ deposition for varying number of ALD cycles. The samples are mounted on a vertical sample holder such that the electron beam is incident perpendicular to the substrate normal [111] and parallel to the $[1\bar{1}1]$ direction. In all the images, we observe that a uniform surface coating is deposited around each NW, and that the NWs are mechanically resilient enough to remain vertical after deposition. There is only a slight variation in NW length (≈ 100 nm for ≈ 2 μm average length wires), suggesting that wire nucleation occurred almost simultaneously on Ge(111) surface and that the growth rates were similar from wire-to-wire. The SiO₂ layer is highly conformal even around the tips of the NWs. The ‘domes’ of SiO₂ surrounding the NWs show a remarkably uniform lateral length scale. Comparing the images from figure A.2(a) (i)–(v), we observe that the oxide thickness around the NWs scales with the number of deposition cycles. A piece of flat Si(100) single crystal kept adjacent to the substrate with NWs, had approximately 3, 12, 45 and 110 nm of SiO₂ deposition after 1, 5, 20 and 50 TBOS cycles, respectively. Differences in apparent dome density result from differences in the original NW density.

Figure A.2(b) (i)–(iv) shows planar SEM images of the same group of NWs after silica PECVD deposition. (i) shows the original NWs. The silica thicknesses in figure A.2(b) (ii)–(iv) corresponds to approximately 200 nm, 500 nm, and 1000 nm, respectively. These images further confirm the finding of uniform oxide deposition by the observation of features of identical diameter. As can be seen in these images, the silica is very conformal even where the NWs are fairly dense and that there is a one-to-one correspondence between ‘domes’ and single NWs. There is some evidence of shadowing effects with this particular process as it can be seen that some of the encapsulated NWs are becoming inversely tapered as a result of non-uniform SiO₂ coating. There is more silica deposition at the tops of the NWs with the PECVD process, and it is not as conformal as the ALD process.

The samples were polished by mounting the wafer piece to a quartz puck with surrounding dummy wafers using parafilm wax. We used an orbital polisher where the sample was placed inverted and rotated at 15 rpm about the carrier as an actuating arm shifted the carrier back and forth along the top of a Suba[®] 500 polyurethane impregnated polyester felt pad from Rohm and Haas which is also rotated at 48 rpm (an orbital polisher). We use a downward force of about 1 kg cm⁻² for about 2 min. One of the other issues is the repeatability and uniformity of CMP. While it is virtually impossible to deterministically remove some given amount of material by CMP, we found that we could use Si₃N₄ layers as a CMP stop layer. When depositing only SiO₂, we found that we could effectively polish the vertical NWs to the thickness of the SiO₂ deposited. The NWs must grown to be longer than the thickness of SiO₂ deposited, and growing NWs so that there is a greater difference between NW height and SiO₂ thickness helps the reliability of the process. The NWs can then be polished fairly reliably to the height of the thickness of the

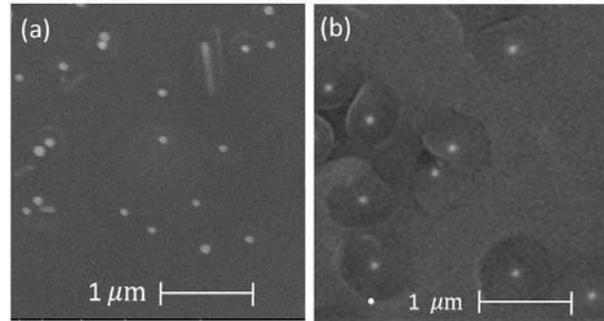


Figure A.3. Comparison of CMP results. (a) Shows a planar SEM picture of a sample with silicon oxide by alternating layer deposition after CMP. (b) Shows a planar SEM sample with PECVD silicon oxide after CMP. The alternating layer oxide allows for better planarization of the sample, while the polishing rate of the PECVD is not as uniform, as the oxide around the NWs tends to polish at a faster rate.

SiO₂ deposited, since there is substantially less material to be removed above this thickness. As an example, we have grown NWs about 1.2 μm in height, deposited 600 nm of SiO₂, and can fairly reliably polish the sample to a thickness of about 600 nm SiO₂.

Figure A.3 shows the main CMP results in comparing ALD oxide and PECVD oxide. Figure A.3(a) shows a sample alternating layer deposition with silicon oxide after CMP. Once the ‘domes’ are polished down to the height of the surrounding oxide, the oxide is polished at a uniform rate. Figure A.3(b) shows a planar SEM sample with PECVD silicon oxide after CMP. The oxide around the NWs tends to polish at a faster rate than the surrounding PECVD oxide and we frequently observe ‘bowl’ structures around the NWs. We believe the stoichiometry of the PECVD oxide that is deposited initially differs from that of the remaining oxide, and thus, tends to polish at a faster rate. In our HF etching tests, we have also found that the oxide around the NWs tends to etch at a faster rate as well, in some cases leaving large empty ‘bowls’ with a freestanding NW in the middle.

Top metal contacts were deposited on the Ge NW samples using a liftoff process. 1 μm of Shipley 3612 photoresist was spun onto the wafer and LDD26W was used for developing the photoresist. We found that the LDD26W developer solution etched the Ge NWs at about 2 nm min⁻¹, which would not sufficiently hinder the deposition process. An O₂ descum process was used 30 s in a plasma etcher, to remove any organics and the sample was dipped in 50:1 HF for 30 s to remove the native oxide before metal deposition. 4 nm of Ti was deposited as a sticking layer, followed by 40 nm of Pd by e-beam evaporation both without substrate heating. The chamber was pumped to $<3 \times 10^{-7}$ Torr using a cryopump before metal deposition. After deposition, the samples were soaked in acetone for 5 min to remove the photoresist on the sample. A variety of different sized Pd pads were put down from (3 μm)² to (1000 μm)² in area.

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