GaAs Enhancement-Mode NMOSFETs Enabled by Atomic Layer Epitaxial La$_{1.8}$Y$_{0.2}$O$_3$ as Dielectric


Abstract—We demonstrate high-performance enhancement-mode (E-mode) GaAs NMOSFETs with an epitaxial gate dielectric layer of La$_{1.8}$Y$_{0.2}$O$_3$ grown by atomic layer epitaxy (ALE) on GaAs(111)A substrates. A 0.5-μm-gate-length device has a record-high maximum drain current of 336 mA/mm for surface-channel E-mode GaAs NMOSFETs, a peak intrinsic transconductance of 210 mS/mm, a subthreshold swing of 97 mV/dec, and an $I_{ON}/I_{OFF}$ ratio larger than $10^7$. The thermal stability of the single-crystalline La$_{1.8}$Y$_{0.2}$O$_3$–single-crystalline GaAs interface is investigated by capacitance–voltage ($C–V$) and conductance–voltage ($G–V$) analysis. High-temperature annealing is found to be effective to reduce $D_{it}$.

Index Terms—Atomic layer epitaxy (ALE), enhancement mode (E-mode), GaAs MOSFET.

I. INTRODUCTION

As the device scaling and performance improving continues, silicon CMOS technology is approaching its fundamental physical limits. Meanwhile, III-V semiconductors have gained more and more attention, as they are promising candidates for replacing silicon owing to their high electron mobility and high saturation velocity [1]–[5]. During the past decades, tremendous efforts have been made to improve the oxide–GaAs interface, which is crucial for device performance [6]–[9]. However, despite some encouraging progress, the surface-channel enhancement mode (E-mode) GaAs NMOSFETs still exhibit relatively low current drivability due to the high interface trap density ($D_{it}$) at the oxide–GaAs interface even on (111)A substrate [9], [10]. In this letter, we demonstrate, for the first time, that, by using atomic layer epitaxy (ALE) [11], [12] to deposit the gate dielectric, high-performance GaAs surface-channel NMOSFETs can be achieved. These devices show low subthreshold slope (SS) around 97 mV/dec and high ON-state current ($I_{ON}$) of 336 mA/mm, which is one order of magnitude higher than that of other reported devices [9], [10]. The systematic study of $C–V$ and $G–V$ characteristics confirms that this novel epitaxy has an excellent quality of interface, and it is thermally stable for the fabrication process of the inversion-mode GaAs NMOSFETs.

II. FABRICATION OF GAAS NMOSFETS

The cross-sectional view of a GaAs(111)A NMOSFET is schematically illustrated in Fig. 1(a). The fabrication started on 2-in GaAs(111)A semi-insulating wafers. The (111)A surface is favorable for GaAs MOSFET since it is difficult to form As–As bonds, which would pin the Fermi level in GaAs [13]. As-received GaAs wafers were first degreased by acetone, methanol, and isopropanol, and then dipped in diluted HCl to remove native oxide. Then, the wafers were soaked in 10% (NH$_4$)$_2$S for 15 min at room temperature for surface passivation. After the sulfur passivation and deionized water rinse, the wafers were quickly transferred into the deposition chamber within less than 1 min for dielectric deposition. La$_{1.8}$Y$_{0.2}$O$_3$ of 7.5 nm was deposited by the ALE in this letter, followed by 6.5-nm Al$_2$O$_3$ serving as a capping layer to prevent La oxide reacting with water in air and/or during the process. The deposition of La$_{1.8}$Y$_{0.2}$O$_3$ film involves precursors of lanthanum tris(N, N'-disopropylformamidinate), yttrium tris(N, N'-disopropyl-acetamidinate) (from the Dow Chemical Company), and H$_2$O, and the deposition of Al$_2$O$_3$ used trimethyl-lalumium and H$_2$O as the precursors. The base pressure of the reactor chamber was 0.3 torr. In each cycle, the exposure...
of the La and Y precursors was 0.003 torr, and the exposure of H<sub>2</sub>O was 0.06 torr. After each H<sub>2</sub>O pulse, the chamber was purged under nitrogen flowing for 80 s to minimize the amount of water and/or hydroxyl groups trapped in the oxide film, as they considerably degrade the crystallinity and the permittivity. A more detailed deposition process is described elsewhere [12]. To fabricate the devices, source and drain regions were selectively implanted with a Si dose of 1 × 10<sup>14</sup> cm<sup>-2</sup> at 30 keV and 1 × 10<sup>14</sup> cm<sup>-2</sup> at 80 keV. Implantation activation was achieved by rapid thermal anneal (RTA) at 860 °C for 15 s in N<sub>2</sub> ambient. The source and drain areas were defined by photolithography and then covered by evaporated Au/Ge/Ni/Au metal stack. After a lift-off process, the RTA at 400 °C for 30 s in 1 atm. pressure of N<sub>2</sub> was performed to form ohmic contacts. The device fabrication process was completed with electron beam evaporation of Ni/Au as gate electrodes, followed by a lift-off process. The fabricated devices have a nominal gate length L<sub>G</sub> varying from 0.5 to 40 μm, while the gate width is fixed at 100 μm. The MOS capacitors were fabricated on p-type (Zn-doped) GaAs(111)A substrates with a doping level of 5–7 × 10<sup>17</sup> cm<sup>-3</sup> and n-type (Si-doped) GaAs(111)A substrates with a doping level of 6–9 × 10<sup>17</sup> cm<sup>-3</sup>. The same oxide stacks of 7.5-nm La<sub>1-x</sub>Y<sub>x</sub>O<sub>2</sub>O<sub>3</sub>/6.5-nm Al<sub>2</sub>O<sub>3</sub> were used. Ni/Au as the top gate metal was used for the capacitor fabrications. Some of the oxide–GaAs stacks were annealed in N<sub>2</sub> prior to gate electrode formation for studying the thermal stability of the oxide–GaAs interface.

III. RESULTS AND DISCUSSION

As shown in Fig. 1(b), the high-resolution transmission electron microscopy (HRTEM) image shows that the single-crystalline La<sub>1.8</sub>Y<sub>0.2</sub>O<sub>3</sub>—single-crystalline GaAs(111)A interface is atomically sharp and flat, and the lattice planes are well aligned. This epitaxial structure of La<sub>1.8</sub>Y<sub>0.2</sub>O<sub>3</sub>/GaAs was further confirmed by high-resolution X-ray diffraction (HRXRD) [12], and the lattice mismatch between La<sub>1.8</sub>Y<sub>0.2</sub>O<sub>3</sub> and GaAs, determined by HRXRD, is ~0.67%. The output characteristics and the transfer characteristics of L<sub>G</sub> = 0.5 μm GaAs(111)A NMOSFET are plotted in Fig. 2(a) and (b), respectively. The gate leakage current density is also plotted in Fig. 2(b). At a gate bias of 5 V and a drain bias of 2 V, a high maximum drain current of 336 mA/mm is achieved, which is a significant improvement of the on-state current compared with the previously reported GaAs (111)A NMOSFETs with amorphous Al<sub>2</sub>O<sub>3</sub> as the gate dielectric [10]. We believe that this is due to the novel high-quality La<sub>1.8</sub>Y<sub>0.2</sub>O<sub>3</sub>–GaAs epitaxial interface that passivates surface dangling bonds on the GaAs surface such that the interface traps are greatly reduced. [11], [12] The peak mobility of these devices is determined to be 310 cm<sup>2</sup>/V·s at an inversion charge density of 2 × 10<sup>12</sup>/cm<sup>2</sup> by split-CV method. It reduces to 230 cm<sup>2</sup>/V·s at 7 × 10<sup>12</sup>/cm<sup>2</sup> inversion charge density. The drive current and the channel mobility could be further enhanced using GaAs buried channel structure [7] or the incorporation of InGaAs higher mobility channel materials [3]–[5]. Our GaAs NMOSFETs also exhibit a high I<sub>ON</sub>/I<sub>OFF</sub> ratio greater than 10<sup>7</sup> (I<sub>OFF</sub> at V<sub>G</sub> = 0.5 V and V<sub>D</sub> = 2 V; I<sub>ON</sub> at V<sub>G</sub> = 2.3 V and V<sub>D</sub> = 2 V). This high I<sub>ON</sub>/I<sub>OFF</sub> ratio is a promising feature for GaAs as compared with InGaAs, since the latter usually suffers from high S/D leakage current as a result of its relatively narrower band gap. The NMOSFETs with any gate length fabricated in this letter (i.e., from 0.5 to 40 μm) consistently show low SS ~ 97 mV/dec, suggesting a low D<sub>it</sub> value of ~3.0 × 10<sup>12</sup>/cm<sup>2</sup>-eV in the midgap using SS = 60 mV/dec (1 + qD<sub>it</sub>/C<sub>ox</sub>). We notice that the gate leakage current increases from ~10<sup>-7</sup> to ~10<sup>-3</sup> A/cm<sup>2</sup> as the gate bias increases from 0 to 4 V, but still, the leakage current is five orders of magnitude lower than the drain current (V<sub>G</sub> = 4 V). Fig. 2(c) shows the effective gate length L<sub>eff</sub> and the series resistance R<sub>SD</sub> extracted by plotting R<sub>CH</sub> versus L<sub>G</sub>, where R<sub>CH</sub> represents the total channel resistance measured from devices with various gate lengths under gate bias from 2.5 to 4 V. R<sub>SD</sub> is determined to be 2.5 Ω·mm, which can be further reduced by optimizing the processes of ion implantation and S/D contact fabrication. ΔL, defined as the difference between the mask gate length L<sub>G</sub> and L<sub>eff</sub>, is estimated to be ~0.2 μm, due to the lateral dopant diffusion caused by high-temperature activation and/or the photolithographic misalignment. As shown in Fig. 2(d), the maximum intrinsic transconductance G<sub>m</sub> of the L<sub>G</sub> = 0.5 μm GaAs NMOSFET is ~210 mS/mm after subtracting R<sub>SD</sub>/2, whereas the maximum extrinsic G<sub>m</sub> is ~138 mS/mm. G<sub>m</sub> can be also improved by reducing the thicknesses of the La<sub>1.8</sub>Y<sub>0.2</sub>O<sub>3</sub> and Al<sub>2</sub>O<sub>3</sub> capping layer. The equivalent oxide thickness is about 4.5 nm.

We further investigate the thermal stability of the oxide–GaAs interface by comparing the C–V and G–V characteristics measured on samples with and without RTA treatment. Fig. 3 summarizes the C–V characteristics of n- and p-type Ni/Al<sub>2</sub>O<sub>3</sub>/La<sub>1.8</sub>Y<sub>0.2</sub>O<sub>3</sub>/GaAs(111)A MOS capacitors. The annealing treatments at 600 °C and 800 °C were both performed in nitrogen ambient for 30 s. For the p-type C–V
b, c, e, and f were annealed in an RTA system for 30 s in nitrogen atmosphere.

We also used the conductance method to extract the \( D_{\text{h}} \) of the novel epitaxial interface. [14] The distributions of \( D_{\text{h}} \) in the GaAs band gap are summarized in Fig. 4. \( D_{\text{h}} \) for both upper- and lower-half band gaps of GaAs is effectively reduced by the high-temperature annealing, which is consistent with the \( C-V \) data shown in Fig. 3. In the lower half of the band gap, which is close to the valence-band edge, \( D_{\text{h}} \) at the position of \( E - E_V = 0.35 \) eV drops from \( 3 \times 10^{12} \) cm\(^{-2} \) \cdot \) eV\(^{-1} \) for the unannealed sample to \( 5.5 \times 10^{11} \) cm\(^{-2} \) \cdot \) eV\(^{-1} \) for the 800 °C and 860 °C annealed samples. This significant reduction of \( D_{\text{h}} \) near the conduction-band edge and also the midgap is the key to realize high-performance surface-channel GaAs NMOSFETs at epitaxial oxide/semiconductor interface.

IV. Conclusion

In summary, we have demonstrated high-performance surface-channel E-mode GaAs(111)A NMOSFETs with ALE La\(_{0.1}\)As\(_{0.9}\)O\(_3\) gate dielectric showing record-high drain current and sub-100-mV/dec subthreshold slope. We believe this high-quality epitaxial structure with excellent interface quality is very promising for future high-speed low-power logic and RF device applications.

**REFERENCES**


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